

SMA Type Female 2Way Divider X 8

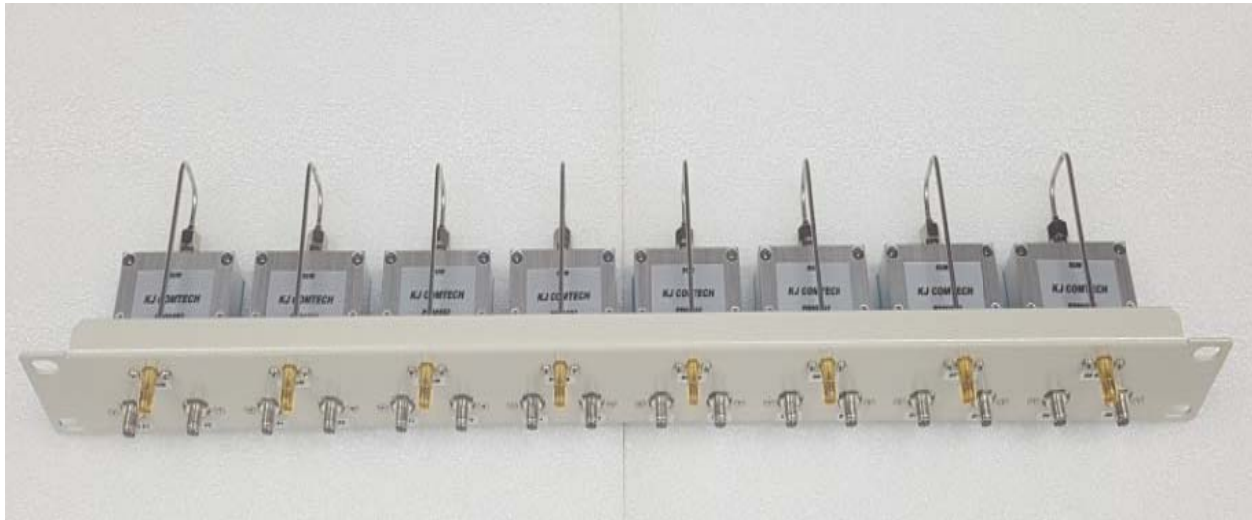


사진 1)

- KJ Comtech Code : PM00029-7/1
- SMA Female

1. Electrical & Mechanical Specification

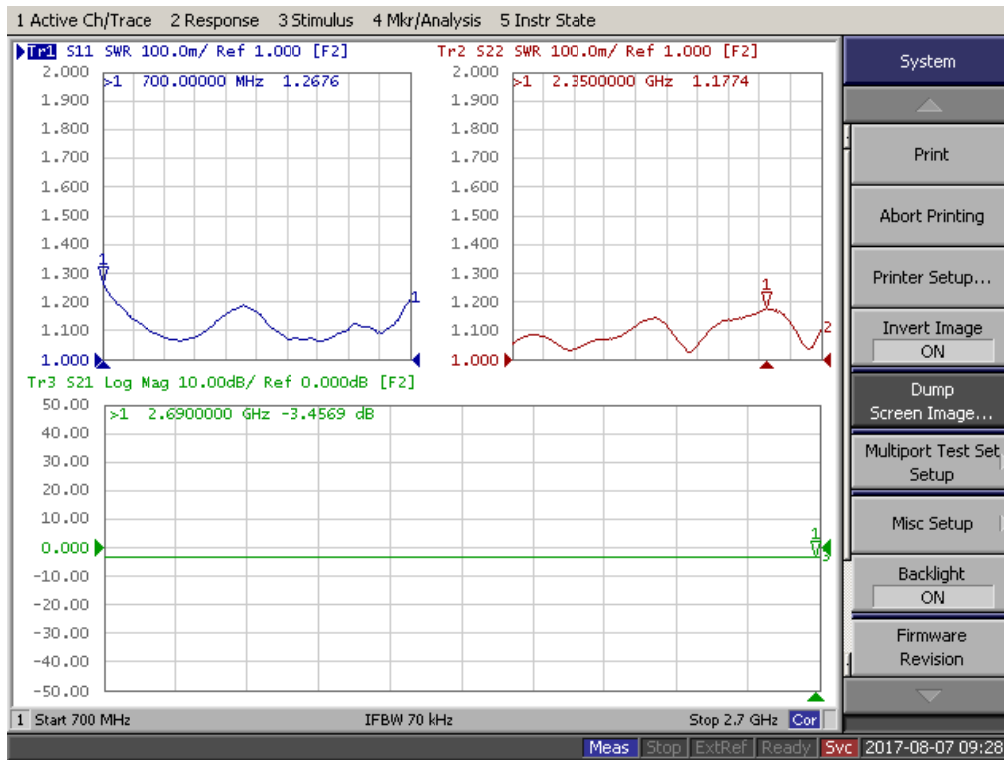
Electrical Specifications	D1~D8 적용
Frequency Range	700~2700MHz
VSWR(Input)	$\leq 1.4 : 1$
Insertion Loss	$\leq 3.7\text{dB}$
Power Handling	1W
Isolation	$\geq 18\text{dB}$
Impedance	50Ω

표1)

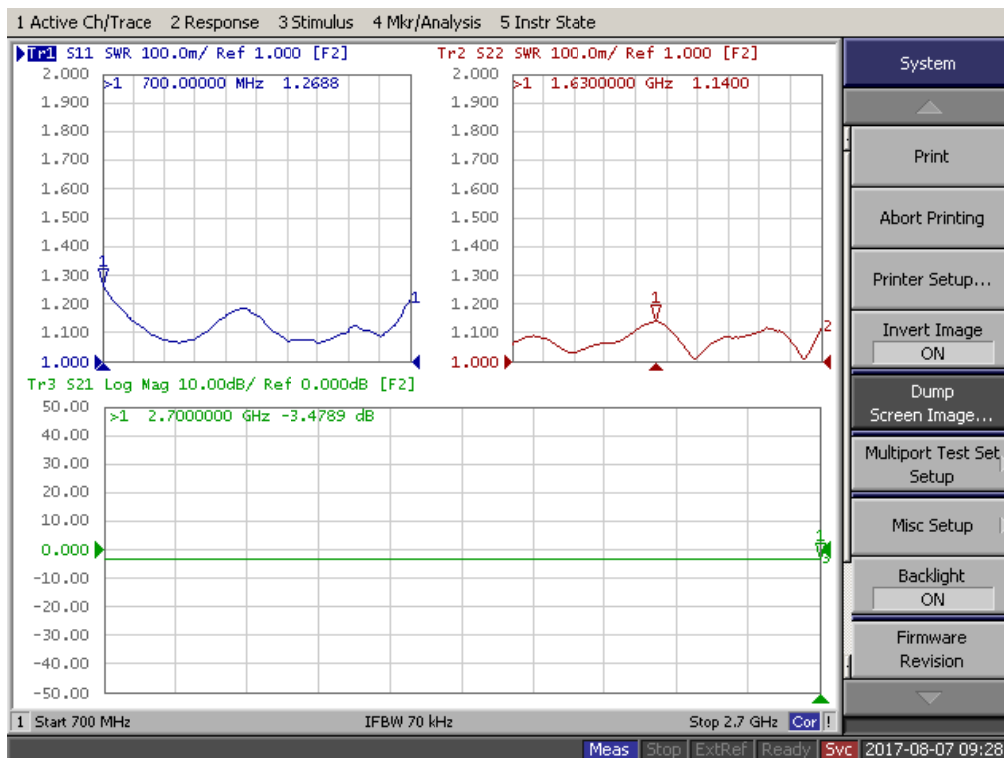
2. SAMPLE1

2.1. RF Data

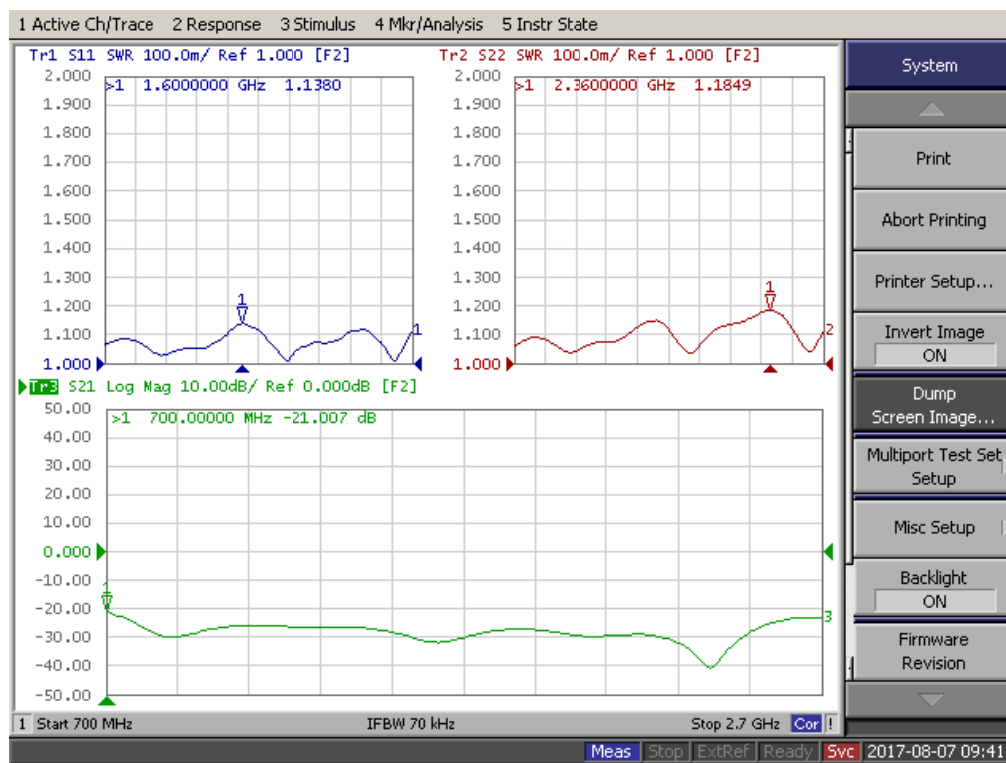
TR1: D1_SUM Port VSWR, TR2: D1_P1 Port VSWR, TR3: (D1_SUM)-(D1_P1) Port Insertion Loss



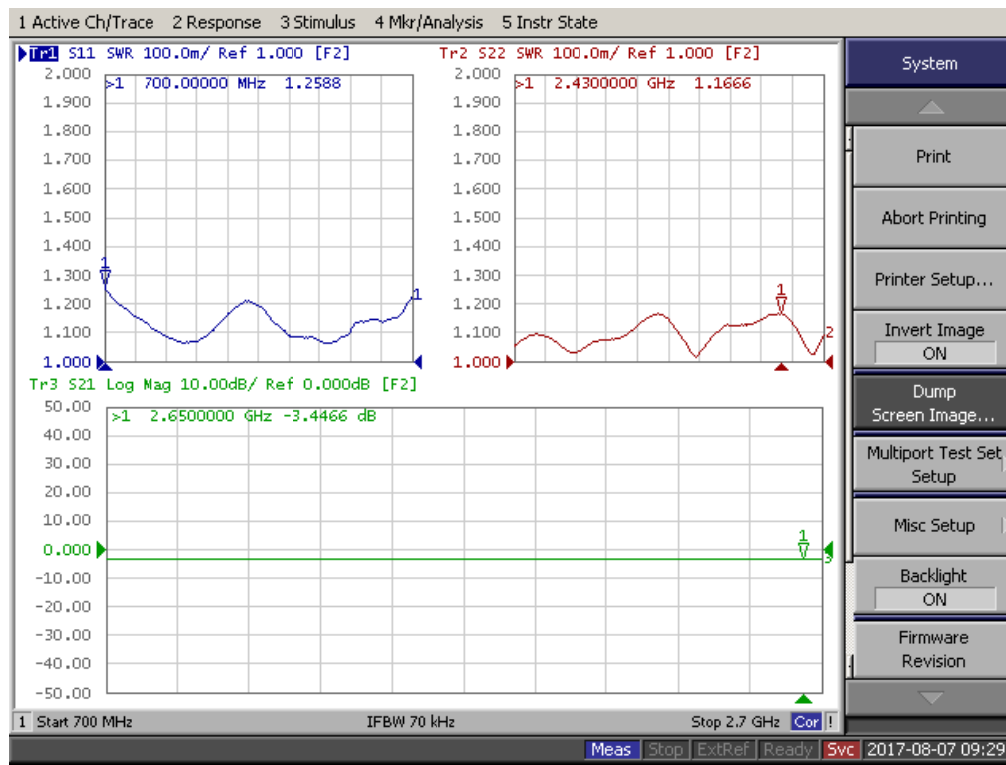
TR1: D1_SUM Port VSWR, TR2: D1_P2 Port VSWR, (D1_SUM)-(D1_P2) Port Insertion Loss



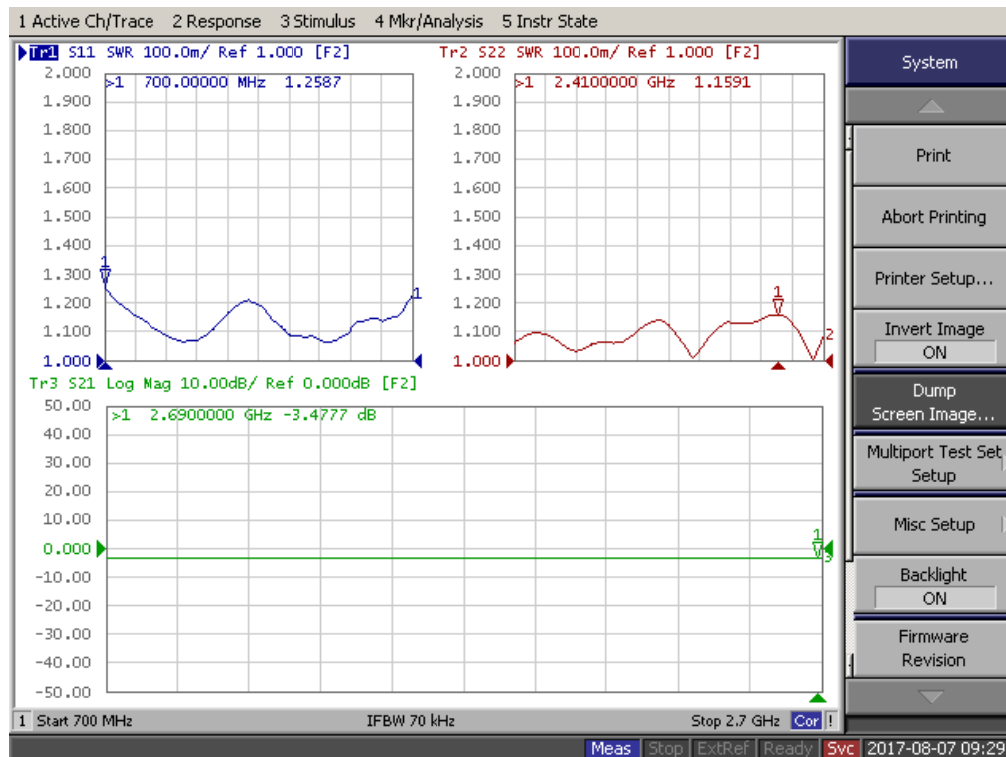
TR1: D1_P1 Port VSWR, TR2: D1_P2 Port VSWR, TR3; (D1_P1)-(D1_P2) Port Isolation



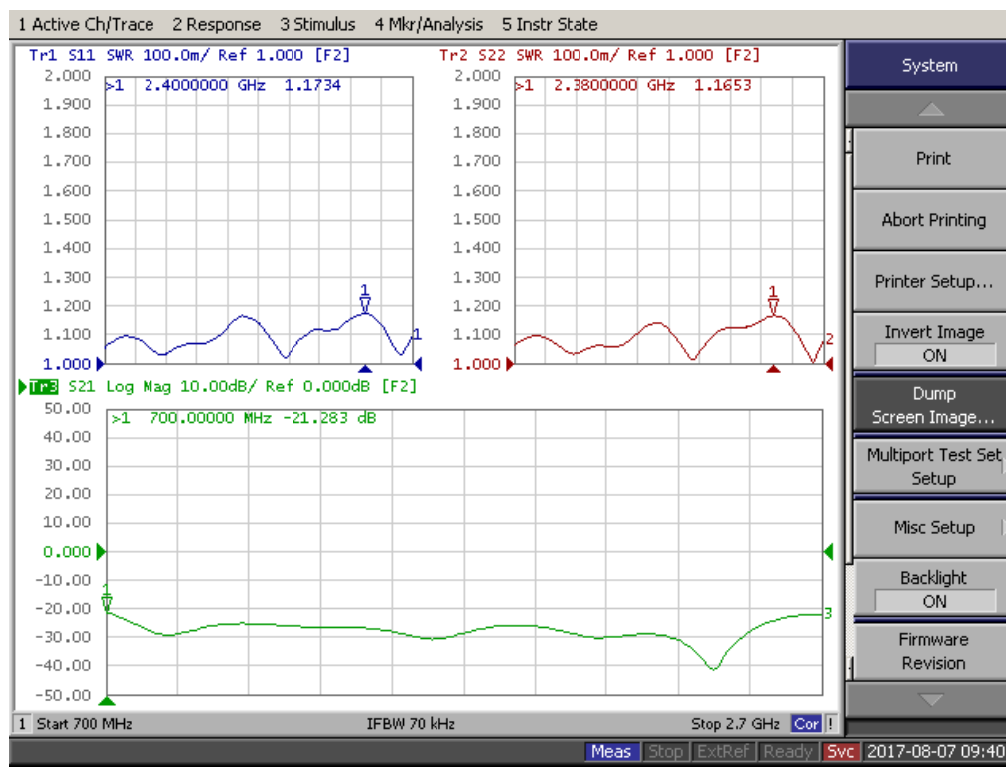
TR1: D2_SUM Port VSWR, TR2: D2_P1 Port VSWR, TR3; (D2_SUM)-(D2_P1) Port Insertion Loss



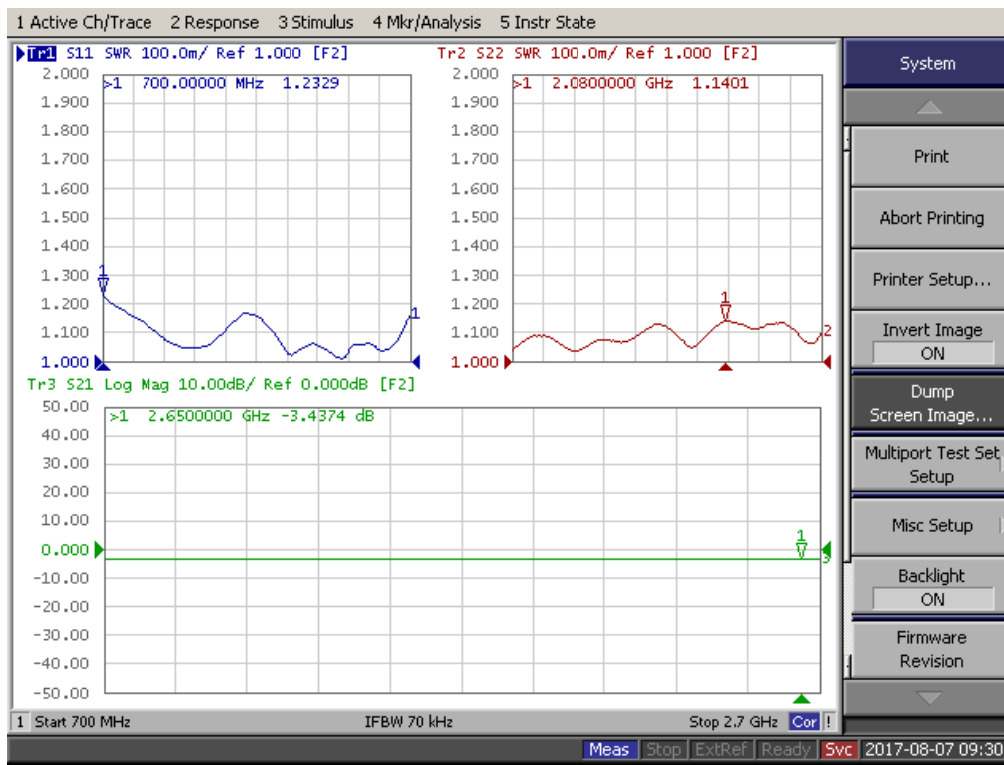
TR1: D2_SUM Port VSWR, TR2: D2_P2 Port VSWR, (D2_SUM)-(D2_P2) Port Insertion Loss



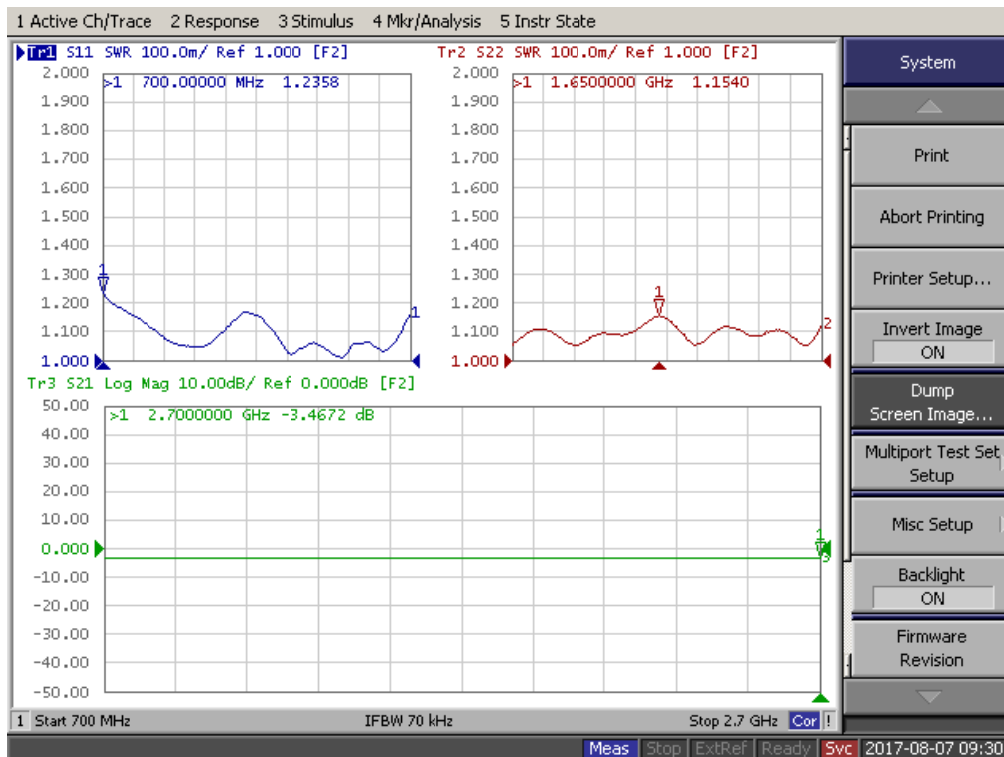
TR1: D2_P1 Port VSWR, TR2: D2_P2 Port VSWR, TR3; (D2_P1)-(D2_P2) Port Isolation



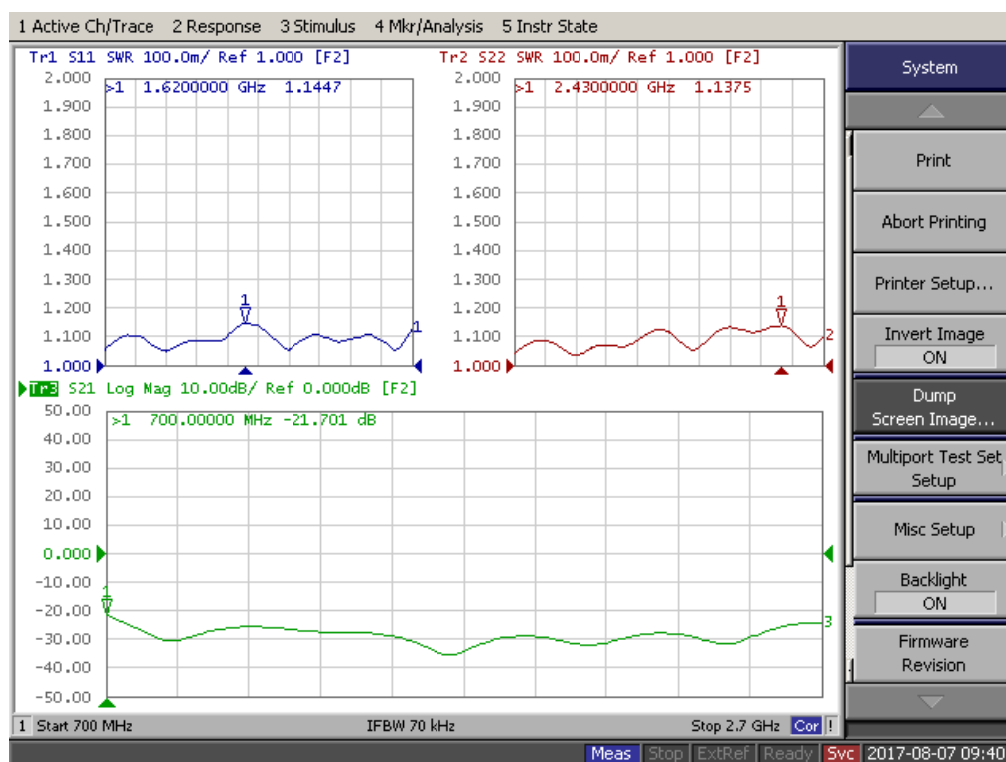
TR1: D3_SUM Port VSWR, TR2: D3_P1 Port VSWR, TR3; (D3_SUM)-(D3_P1) Port Insertion Loss



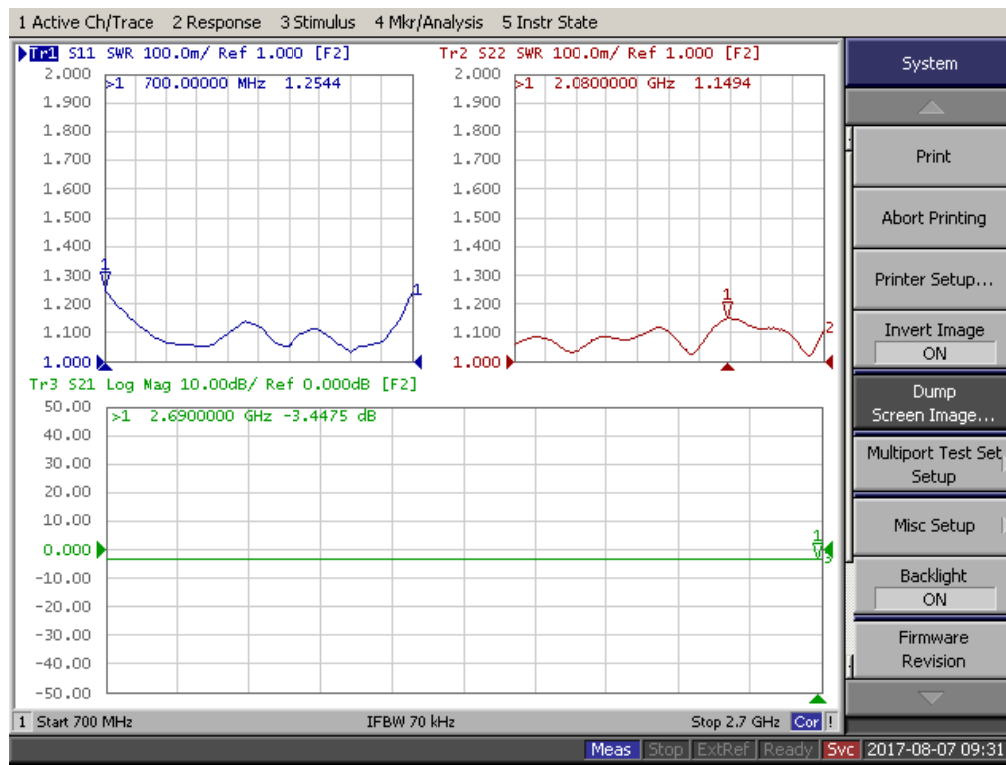
TR1: D3_SUM Port VSWR, TR2: D3_P2 Port VSWR, (D3_SUM)-(D3_P2) Port Insertion Loss



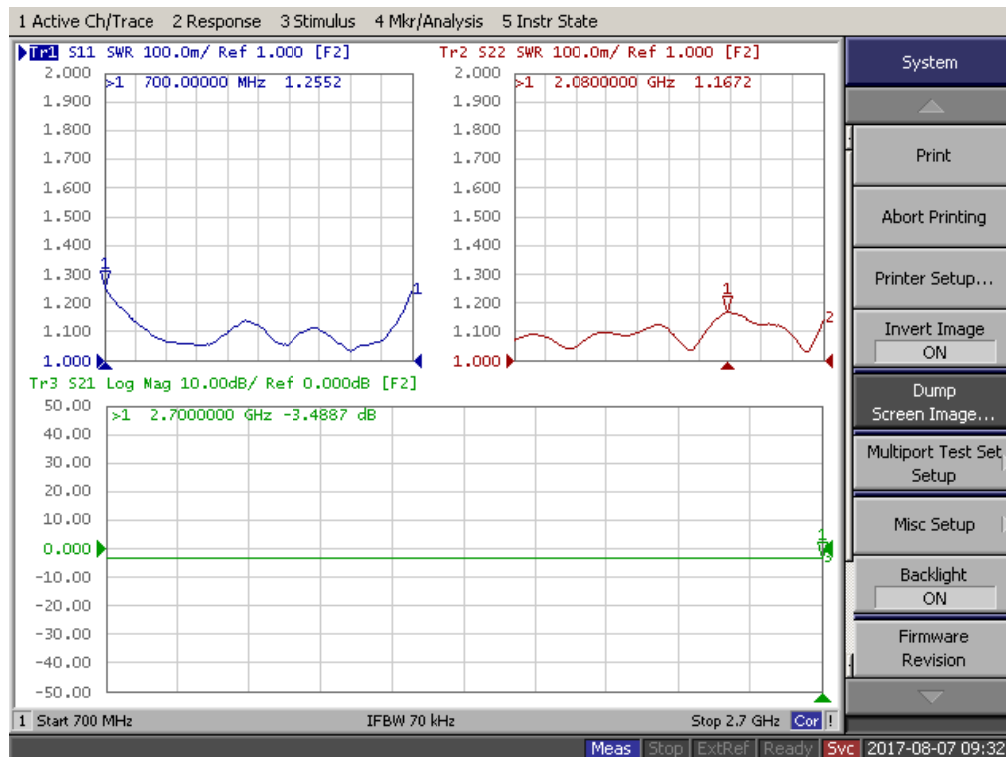
TR1: D3_P1 Port VSWR, TR2: D3_P2 Port VSWR, TR3; (D3_P1)-(D3_P2) Port Isolation



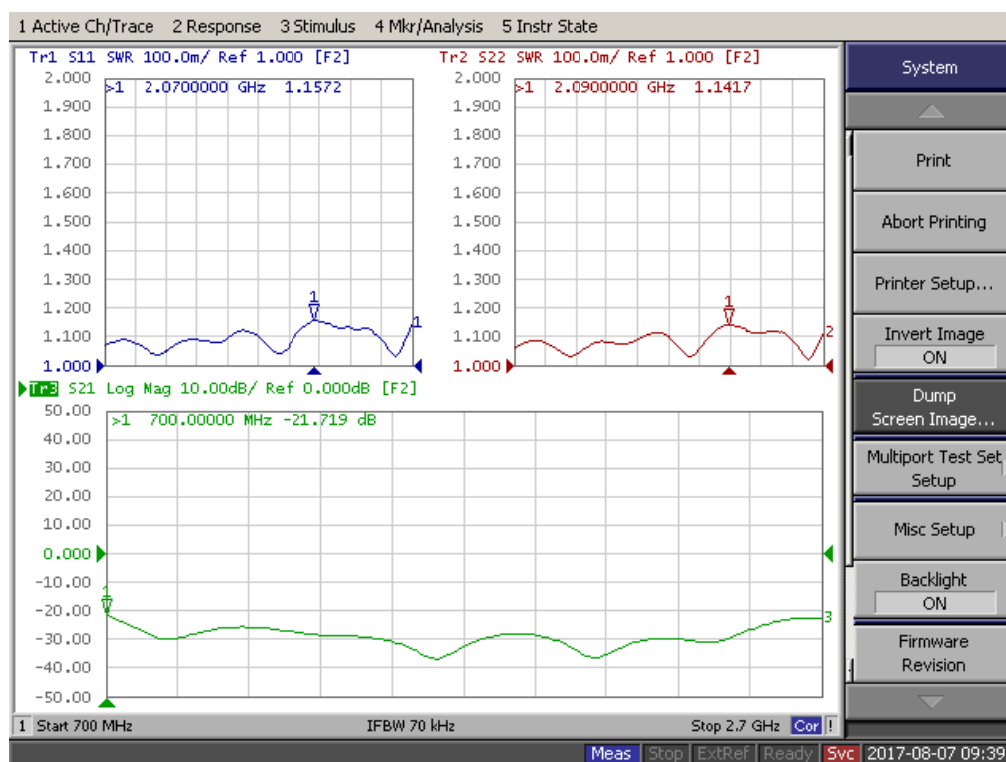
TR1: D4_SUM Port VSWR, TR2: D4_P1 Port VSWR, TR3; (D4_SUM)-(D4_P1) Port Insertion Loss



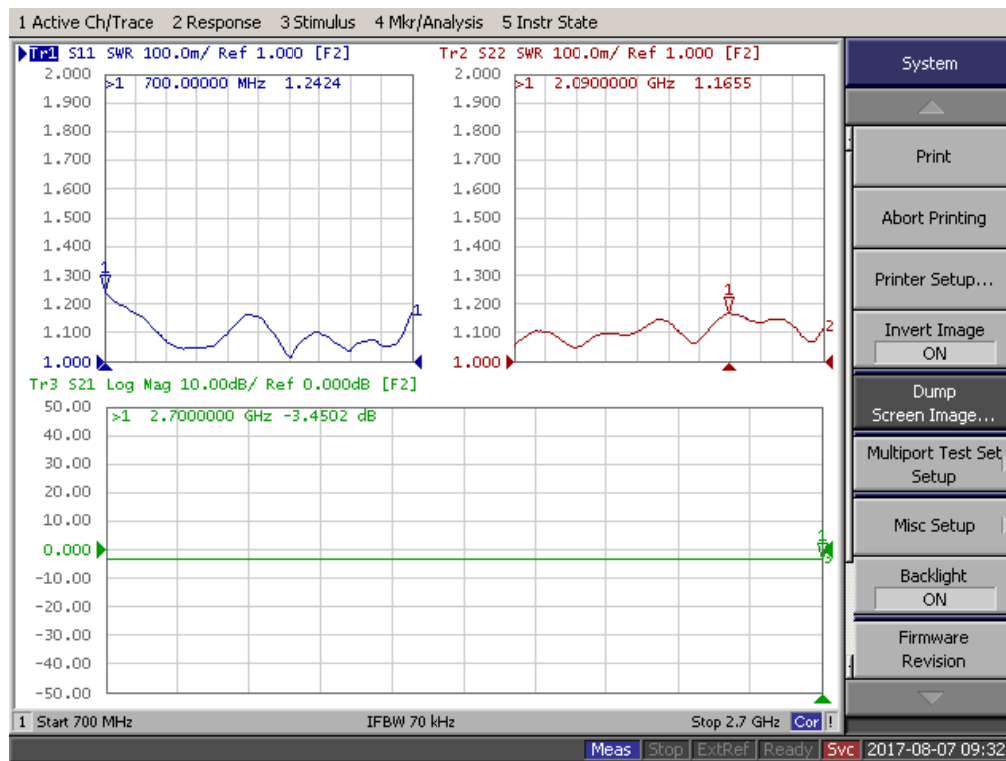
TR1: D4_SUM Port VSWR, TR2: D4_P2 Port VSWR, (D4_SUM)-(D4_P2) Port Insertion Loss



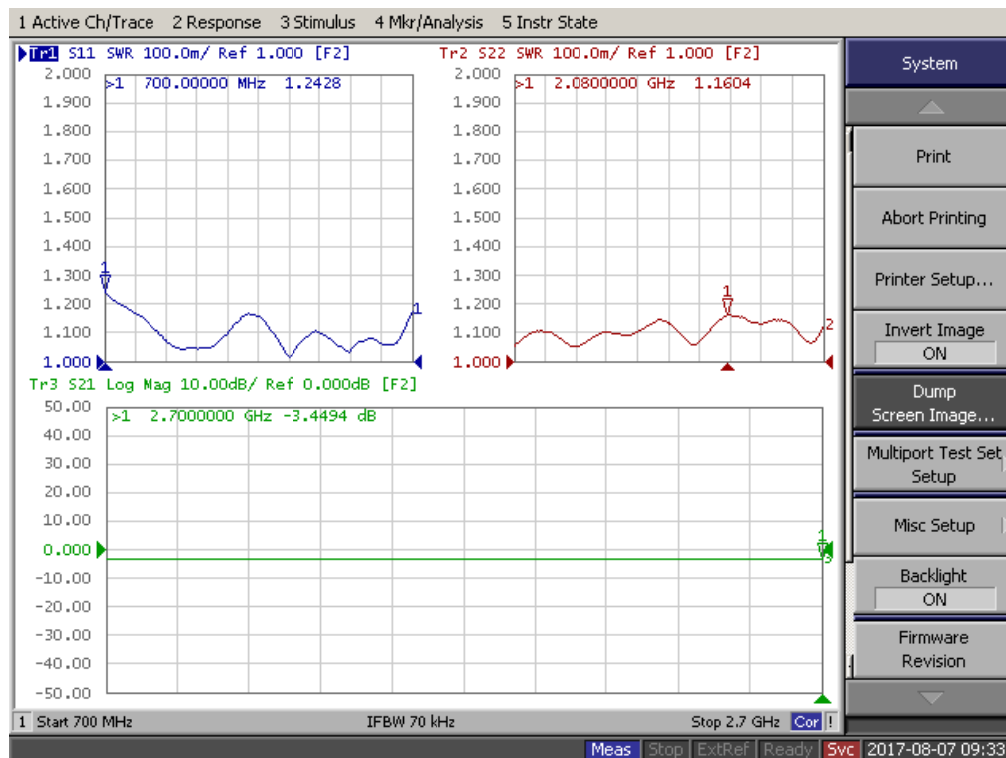
TR1: D4_P1 Port VSWR, TR2: D4_P2 Port VSWR, TR3; (D4_P1)-(D4_P2) Port Isolation



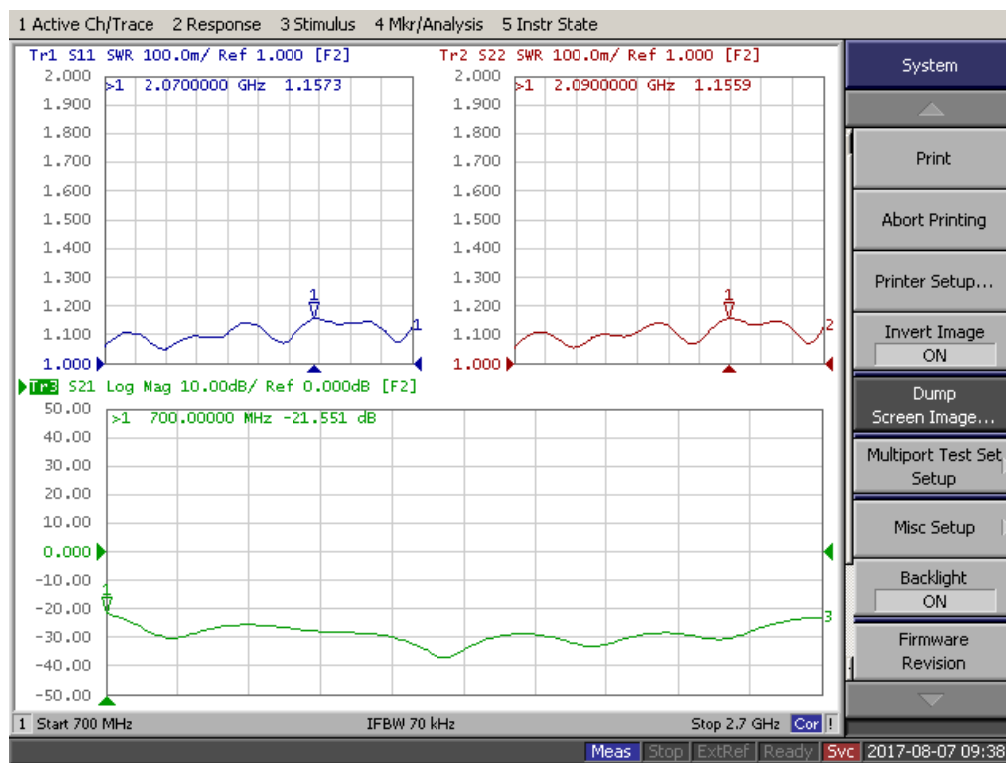
TR1: D5_SUM Port VSWR, TR2: D5_P1 Port VSWR, TR3; (D5_SUM)-(D5_P1) Port Insertion Loss



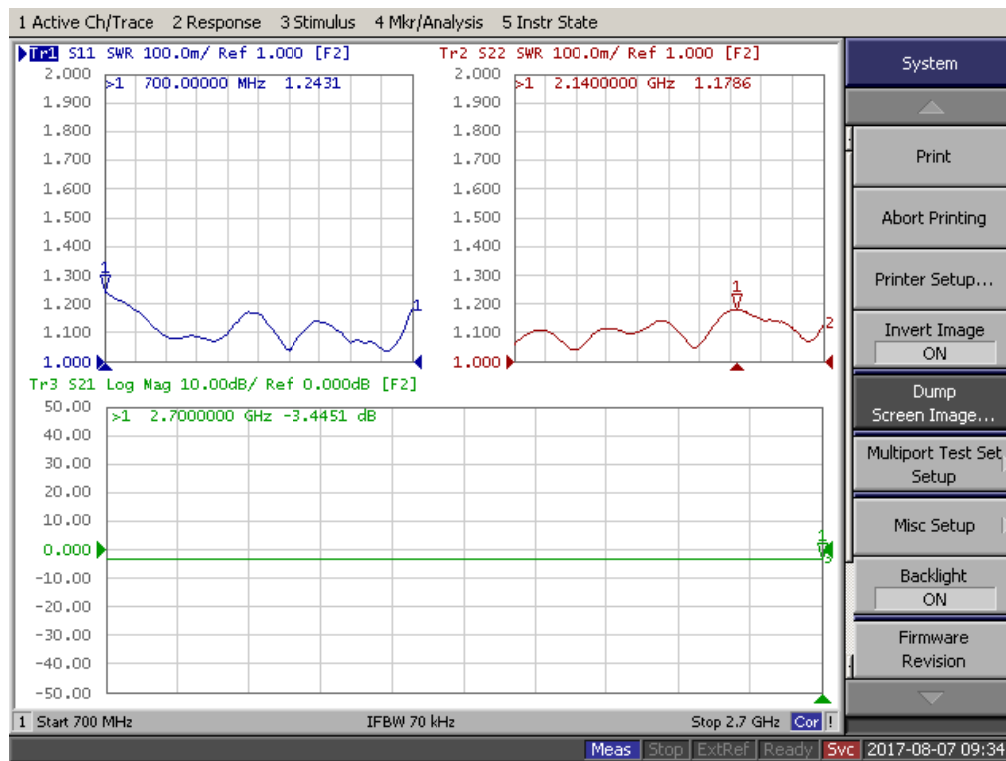
TR1: D5_SUM Port VSWR, TR2: D5_P2 Port VSWR, (D5_SUM)-(D5_P2) Port Insertion Loss



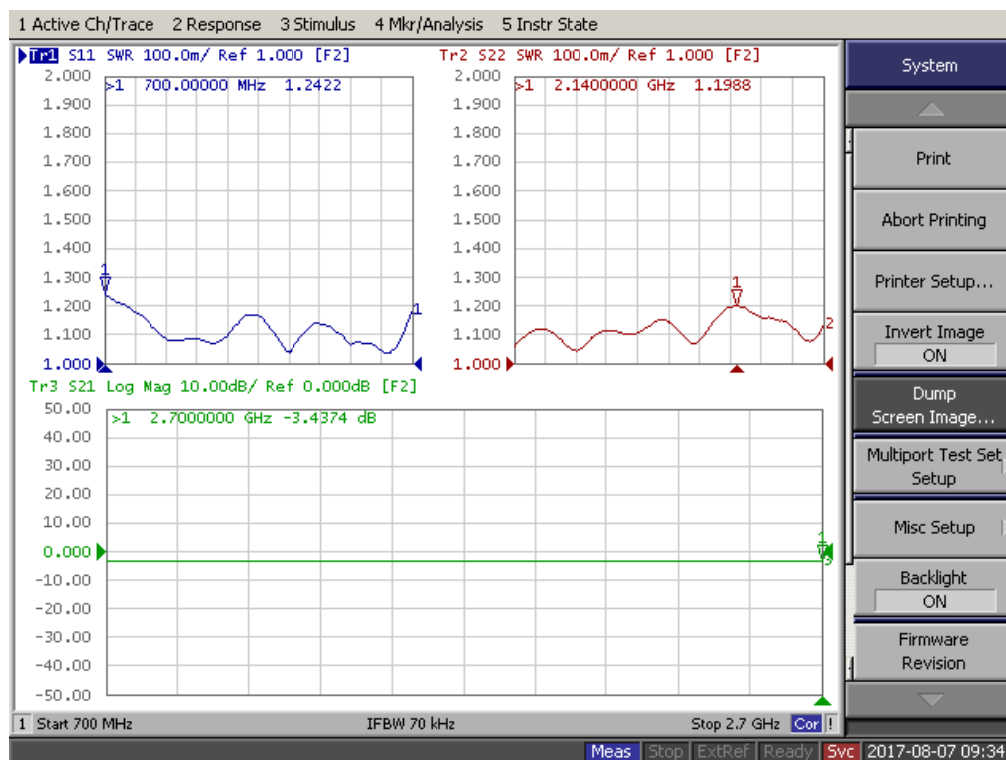
TR1: D5_P1 Port VSWR, TR2: D5_P2 Port VSWR, TR3; (D5_P1)-(D5_P2) Port Isolation



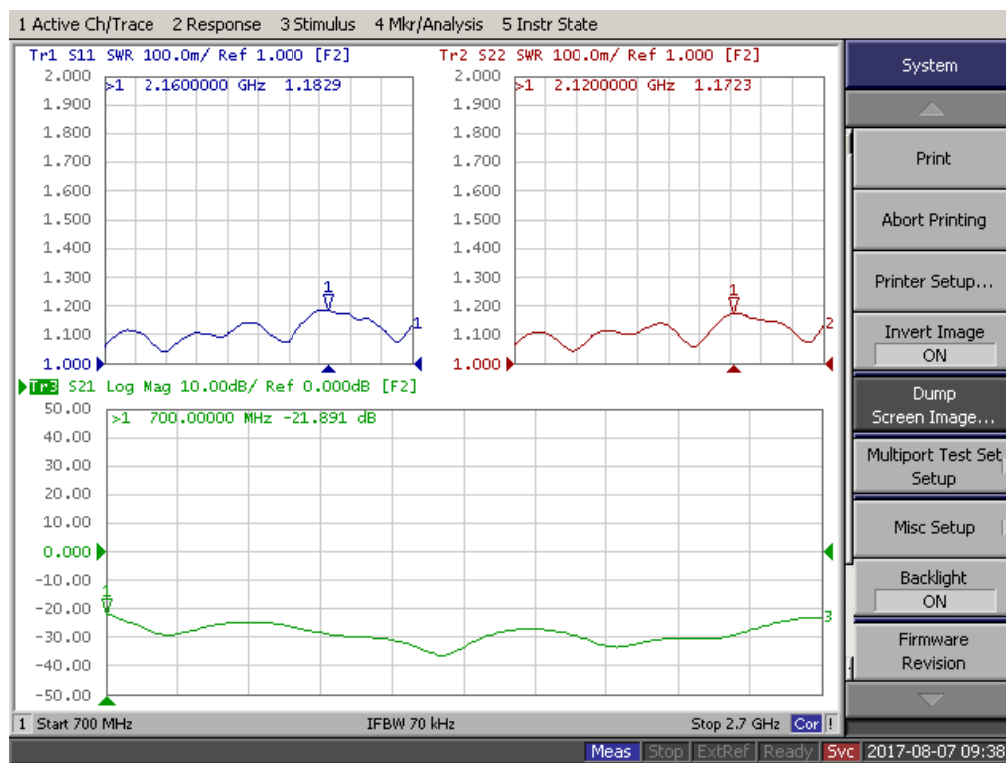
TR1: D6_SUM Port VSWR, TR2: D6_P1 Port VSWR, TR3; (D6_SUM)-(D6_P1) Port Insertion Loss



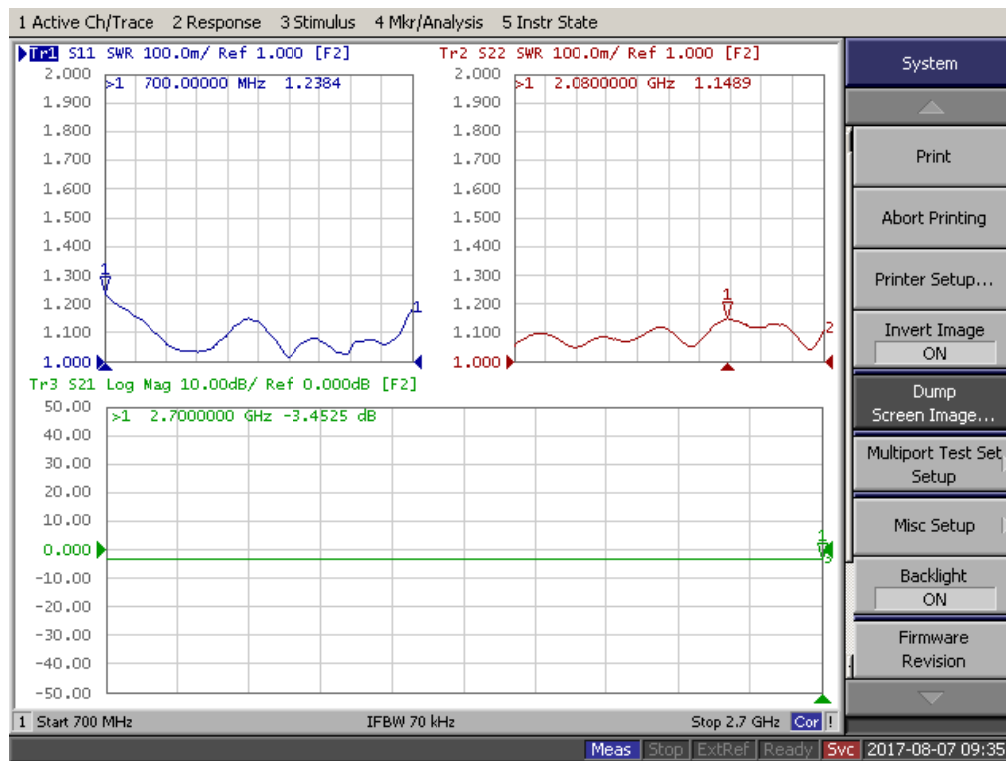
TR1: D6_SUM Port VSWR, TR2: D6_P2 Port VSWR, (D6_SUM)-(D6_P2) Port Insertion Loss



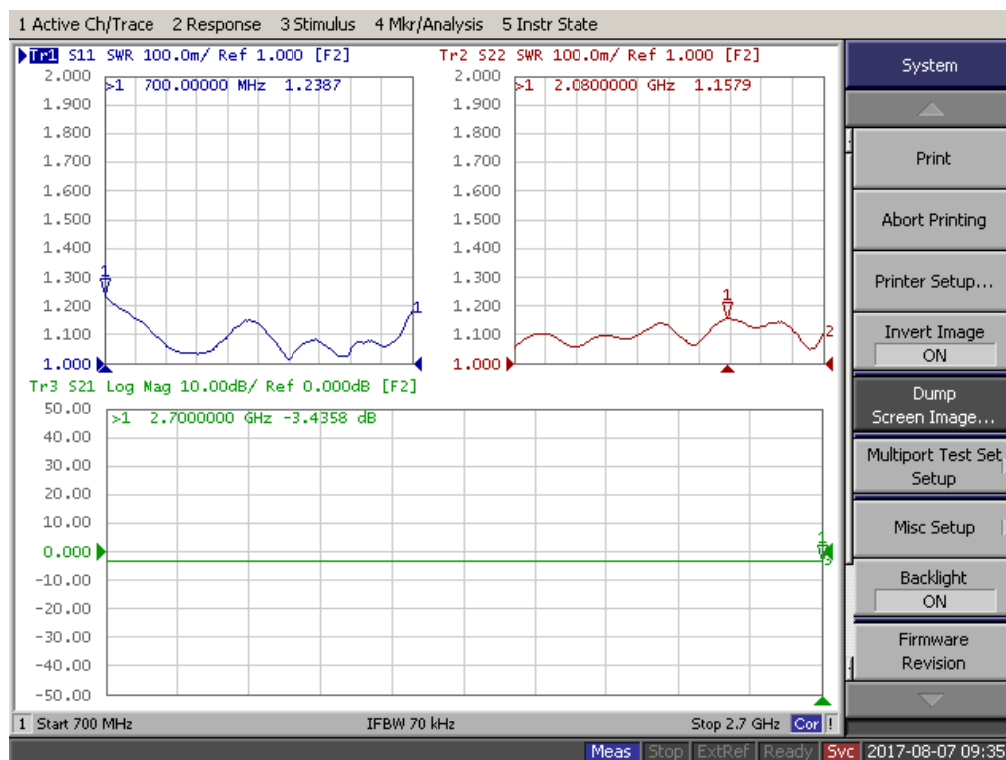
TR1: D6_P1 Port VSWR, TR2: D6_P2 Port VSWR, TR3; (D6_P1)-(D6_P2) Port Isolation



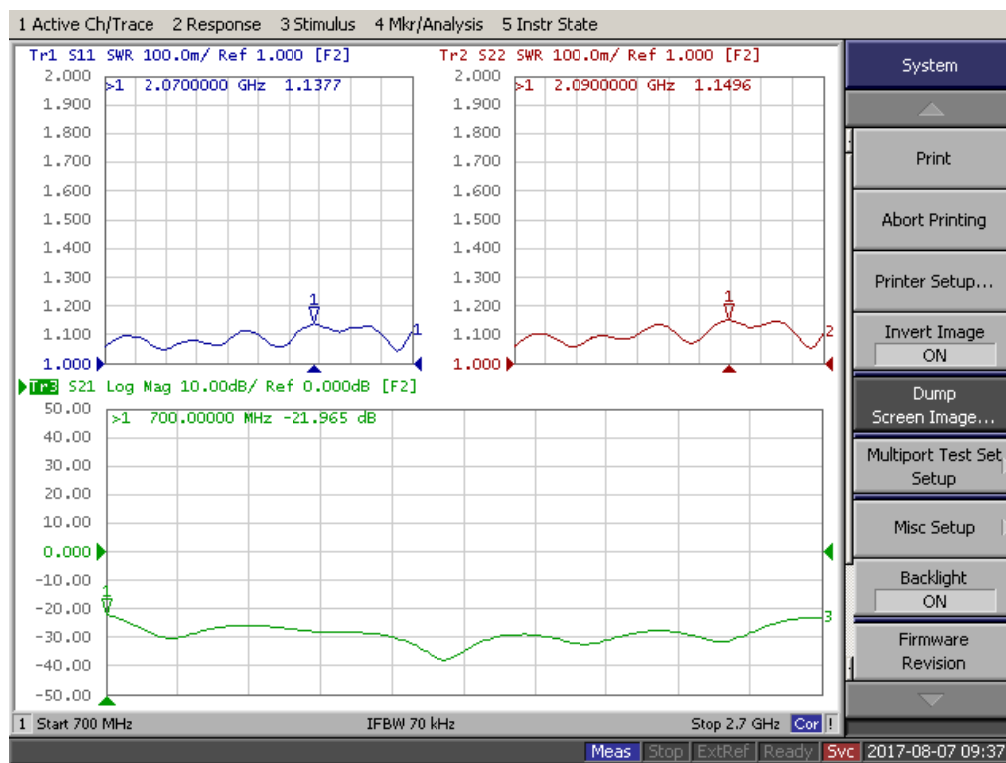
TR1: D7_SUM Port VSWR, TR2: D7_P1 Port VSWR, TR3: (D7_SUM)-(D7_P1) Port Insertion Loss



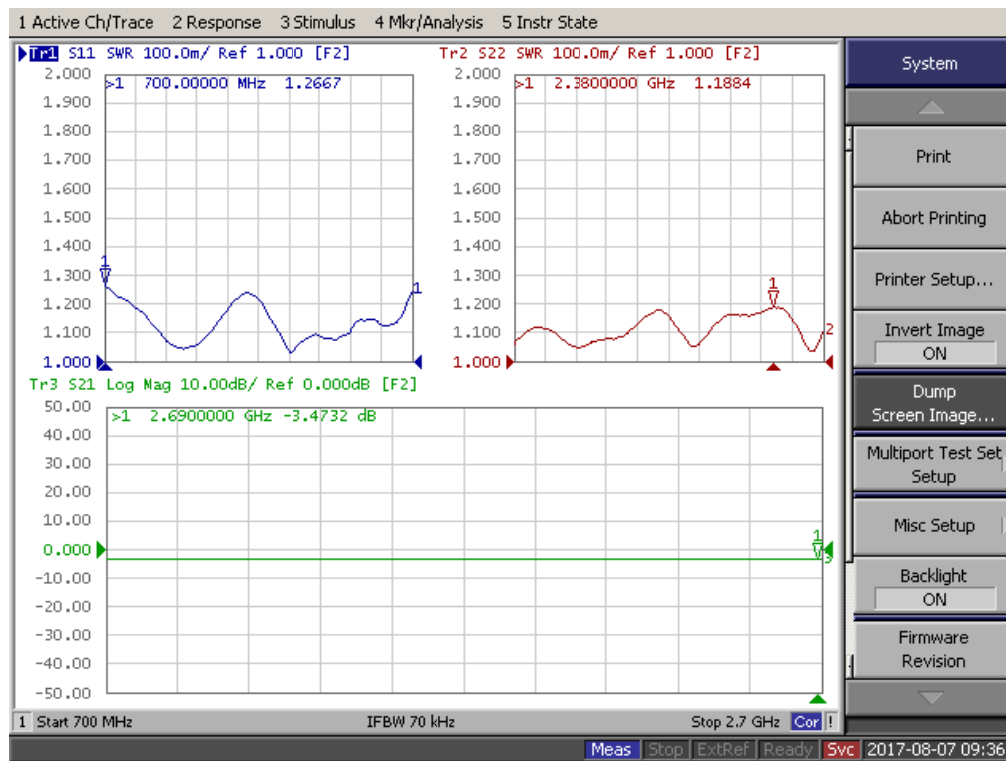
TR1: D7_SUM Port VSWR, TR2: D7_P2 Port VSWR, (D7_SUM)-(D7_P2) Port Insertion Loss



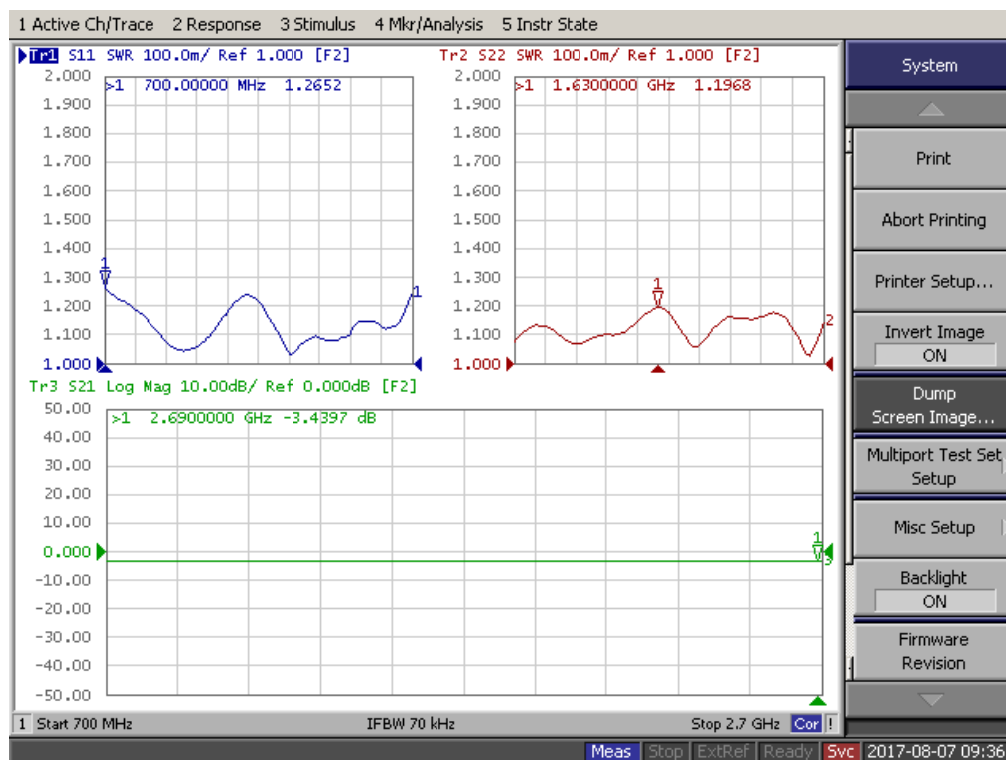
TR1: D7_P1 Port VSWR, TR2: D7_P2 Port VSWR, TR3; (D7_P1)-(D7_P2) Port Isolation



TR1: D8_SUM Port VSWR, TR2: D8_P1 Port VSWR, TR3: (D8_SUM)-(D8_P1) Port Insertion Loss



TR1: D8_SUM Port VSWR, TR2: D8_P2 Port VSWR, (D8_SUM)-(D8_P2) Port Insertion Loss



TR1: D8_P1 Port VSWR, TR2: D8_P2 Port VSWR, TR3; (D8_P1)-(D8_P2) Port Isolation

